REMARKS

In response to the Office Action mailed September 30, 2003, Applicants respectfully request reconsideration. To further the prosecution of this case, amendments and arguments are submitted herewith.

Claims 1-7 were previously pending in this application. By this amendment, claims 6 and 7 have been amended for the sole purpose of clarification, and not to overcome any art of record. New claims 8-30 have been added to further define Applicants' contribution to the art. As a result, claims 1-30 are pending for examination, with claims 1, 4, 8 and 21 being independent claims. No new matter has been added.

Applicants note with appreciation the indicated allowability of dependent claim 6 if rewritten in independent form. However, claim 6 remains in dependent form for the reasons discussed below.

I. Objections to the Drawings

Figures 1-5 have been amended to include the legend "Prior Art." These amendments are believed to overcome the objection in paragraph 1 of the Office Action.

In paragraph 2 of the Office Action, an objection is raised concerning Figure 6A and the term "CK+." Applicants respectfully direct the Examiner's attention to Figure 6A, in which the y-axis is labeled with "CK+". In light of the above-described amendments and arguments, Applicants respectfully request that the objections to the figures be withdrawn.

II. Claim Rejections

Claims 1-5 and 7 stand rejected under 35 U.S.C. §103(a). Applicants respectfully traverse these rejections.

Claims 1 and 4 stand rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over U.S. Patent No. 6,008,746 to White, and further in view of U.S. Patent No. 4,242,754 to DePouilly et al. (hereinafter DePouilly). Applicants respectfully traverse this rejection.

A. Discussion of White

White teaches a method and apparatus for decoding noisy, intermittent data, such as Manchester encoded data. Figure 5 shows an electrical schematic block diagram of a timing recovery and decoding system taught by White (Col. 6, lines 4-7). The input line 40 is connected to a multi-mode input circuit 41 (col. 9, lines 51-55). A test mode control circuit 55, and a transition detector 45 are also included (col. 9, lines 51-59). A sample circuit 120 is connected to the mode control circuit 55. An oscillator 35 is connected to a transition counter 75 (col. 10, lines 53-58). Transition counter 75 is connected to divide-by-2 circuit 105 (col. 11, lines 29-31).

In operation, Manchester encoded data is input on input line 40 to the multimode input circuit 41 (col. 9, lines 51-55). An example of a Manchester data stream 10 is shown in Figure 1, and includes both upward and downward transitions (col. 5, lines 51-54). The output of the multimode input circuit 41 is sent on line 42 to mode control circuit 55 (col. 9, lines 55-61). Mode control circuit 55 controls whether or not to supply the rest of the circuit with the input signal or with a test signal (col. 9, lines 55-61). The transition detector 45 generates a pulse (M2DAT) for each transition of the signal on line 42 (col. 10, lines 25-29). A detailed illustration of transition detector 45 is shown in Figure 7. The signal M2DAT from the transition detector 45 is sent on line 83 to transition counter 75 (col. 10, lines 53-58). Transition counter 75 also receives a clock signal on line 87 from oscillator 35 (col. 11, lines 8-13). The output 100 of transition counter 75 represents a division of the clock pulses provided by oscillator 35 (col. 11, lines 8-15), and is connected to divide-by-2 circuit 105 (col. 11, lines 29-31). Figure 9 shows a detailed illustration of divide-by-2 circuit 105. The divide-by-2 circuit contains a D-type flip-flop 106 that receives the signal on output line 100 from transition counter 75 (col. 11, lines 31-34). The divide-by-2 circuit 105 operates to divide the divided clock pulses on line 100 by two, thus generating a sample command signal that is output on line 117 to sampling circuit 120 (col. 11, lines 43-45). When the signal on line 117 goes high the sample circuit 120 samples the Manchester data MDAT on line 127 (col. 11, line 65-col. 12, line 3; col. 12, lines 17-21).

B. Discussion of DePouilly

DePouilly teaches a clock recovery system for a data receiver (Abstract). A pulse train of data will be sent from a transmitter to a receiver (col. 1, lines 12-14). The receiver also receives a clock (col. 1, lines 24-28). The system of DePouilly allows the receiver to acquire the data signal at the correct time (col. 1, lines 21-23).

Figure 1 shows a circuit diagram of a clock recovery system taught by DePouilly (col. 1, lines 65-66). A gate 1 receives a data signal REC+ (col. 2, lines 6-8). The output of gate 1 is connected to an input of AND gate 2 (col. 1, lines 6-8). An output of the first J-K flip-flop 6 is connected to the second input of AND gate 2 (col. 2, lines 8-11). A second J-K flip-flop 5 is also provided, as well as first and second shift registers 3 and 4, respectively (col. 1, lines 11-20). The CLR input of flip-flop 5 and flip-flop 6 receives a resetting signal RAZ- (col. 2, lines 42-45). A clock signal H+ is fed to a gate 7 (col. 2, lines 14-16 and 31-32). The recovered clock signal CPA of the system is obtained at output Q of J-K flip-flop 5 (col. 2, lines 39-41).

In operation, the clock signal H+ is sent to the input of gate 7 and to the input CK of flip-flop 5 and flip-flop 6 (col. 2, lines 14-16, lines 50-56; Figure 2). The local clock signal H- is present at the output of gate 7 (col. 2, lines 14-16; Figure 2). Signal H- is sent to inputs CK on shift registers 3 and 4 (col. 2, lines 50-56). A data signal REC+ is received by gate 1 (col. 2, lines 6-8). The first signal pulse REC+ triggers the recovered clock signal CPA which is generated by flip-flop 5 (col. 4, lines 12-16). Signal CPA is thus synchronized to the data with an accuracy of one period of the clock signal H (col. 3, lines 42-45). The recovered clock signal CPA will remain high until it is reset using a resetting pulse RAZ- (col. 4, lines 12-16). DePouilly teaches that the signal RAZ- may be output by a shift register that counts the pulses for each pulse train (col. 4, lines 17-20).

C. The Combination Of White and DePouilly Is Improper

Applicant respectfully submits that the asserted combination of White and DePouilly is improper. With respect to claim 1, the only motivation for combining the two references stated on page 3 of the Office Action is that "[i]t would have been obvious to one of ordinary skill in the art to utilize one of the complementary signals (the data portion) to reset the flip-flop in order to help reduce synchronization errors." Applicants respectfully disagree. As discussed above,

DePouilly teaches a method of resetting flip-flops using a signal RAZ-, which "can be generated, for example, by means of a shift register which counts the pulses transmitted over the link for each pulse train and which sends a resetting pulse after the last data signal pulse" (col. 4, lines 17-20). There is no teaching of a similar signal in White. The flip-flop 106 shown in Figure 9 of White is reset by signal 107, which occurs "when two positive edges of the divided clock pulses on line 100 have occurred between any two successive Manchester data transition indicating pulses on line 85" (col. 11, lines 45-49). Thus, the operation of White depends on this nature of the resetting signal on line 107. Substituting signal RAZ- of DePouilly for signal 107 of White would alter the function of White from its intended purpose. Furthermore, it is not clear that such a substitution would achieve the end result of the asserted motivation, i.e. "to help reduce synchronization errors." For at least these reasons the combination is improper.

D. Claim 1 Patentably Distinguishes Over the Combination of White and DePouilly

Claim 1 recites a method for regenerating a clock signal based on a flip-flop and on two complementary signals at the clock rate. Claim 1 further requires the flip-flop being connected as a divider by two of a combination of shaping signals each translating a direction, respectively rising or falling, of the edges of one of the complementary signals, wherein one of said shaping signals is used to reset the flip-flop.

White does not teach or suggest several limitations of claim 1. Contrary to the assertion on page 2 of the Office Action, White does not teach or suggest a method for regenerating a clock signal based on a flip-flop and on two complementary signals at the clock rate. The two signals of White referred to in the Office Action, data and clock, are not two complementary signals at the clock rate. The clock signal produced by oscillator 35 of White, and the data signal present on input line 40 are not complements of each other, but rather are independent. Furthermore, the data signal on line 40 is not at the clock rate, but rather depends on the nature of the data. Therefore, the data and clock signals of White do not meet the limitations of the claimed two complementary signals at the clock rate.

Secondly, claim 1 requires that the flip-flop be connected as a divider by two of a combination of shaping signals each translating a direction, respectively rising or falling, of the edges of one of the complementary signals. Contrary to the assertion on pages 2 and 3 of the

Office Action, White does not teach or suggest such a feature. Since White does not teach or suggest complementary signals, as discussed above, he also does not disclose shaping signals.

Moreover, as correctly noted in the Office Action, White does not teach or suggest the limitation of claim 1 wherein one of said shaping signals is used to reset the flip-flop. Thus, claim 1 clearly distinguishes over White.

DePouilly fails to disclose the limitations not found in White. DePouilly does not teach or suggest a method for regenerating a clock signal based on a flip-flop and on two complementary signals at the clock rate. DePouilly does not teach or suggest the flip-flop being connected as a divider by two of a combination of shaping signals. The flip-flops 5 and 6 of DePouilly are not connected as divider by two flip-flops, and do no receive the claimed shaping signals. Furthermore, DePouilly does not disclose a method wherein one of said shaping signals is used to reset the flip-flop. The flip-flops 5 and 6 of DePouilly are reset by signal RAZ-, which is not equivalent to the claimed shaping signals. If RAZ- were equivalent to the claimed shaping signals, then the flip-flops of DePouilly would need to be in a divide-by-two configuration of some combination of signals including RAZ-. This is obviously not the case, and for at least this reason the claimed shaping signals cannot be read on DePouilly's RAZ- signal.

Thus, it has been demonstrated that both White and DePouilly lack several of the same limitations of claim 1. The claimed invention clearly distinguishes over any combination of White and DePouilly. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) is respectfully requested.

E. Claim 4 Patentably Distinguishes Over the Combination of White and DePouilly

Claim 4 recites a circuit for regenerating a clock signal based on two complementary signals by means of a D-flip-flop, a clock input of which receives the result of a logic combination of two shaping signals resulting from a filtering of the respective rising edges of the complementary signals. Claim 4 further recites the limitation wherein a reset input of the flip-flop receives one of said shaping signals. As discussed above in relation to claim 1, the claimed invention clearly distinguishes over any combination of White and DePouilly. Accordingly, Applicants respectfully request that the rejection of claim 4 under 35 U.S.C §103(a) be withdrawn. Claims 5-7 depend from claim 4 and are allowable for at least the same reasons.

III. New Claims

Claims 8-30 have been added to further define Applicants' contribution to the art.

Claim 8 recites a clock signal regeneration circuit. The circuit comprises a first input for a clock signal and a second input for an inverted clock signal. The circuit further comprises logic to shape the clock signal into a first signal and the inverted clock signal into a second signal, a flip-flop, and means for setting an initial state of the flip-flop after each alternate edge of the second signal.

Support for the claim can be found, for example in Figures 3, 5 and 7, and the corresponding discussion. As a non-limiting example, the first input and second input may read on the inputs to circuit 34 in Figure 3. The claimed logic may read on the logic in Figure 5, for example, with the claimed first signal reading on the output of inverter 41 and the claimed second signal reading on the output of inverter 42. The claimed flip-flop may read on the flip-flop 40', shown in Figure 7. The means for setting an initial state of the flip-flop after each alternate edge of the second signal may, for example, read on the reset input of the flip-flop 40'.

Claim 8 distinguishes over the combination of White and DePouilly for reasons similar to those already discussed in connection with claims 1 and 4. Claims 9-20 depend from claim 8 and are allowable for at least the same reasons.

Claim 21 recites a method of regenerating a clock signal, comprising acts of shaping a clock signal into a first signal and an inverted clock signal into a second signal, and setting an initial state of a flip-flop after each alternate edge of the second signal, wherein the flip-flop is coupled to the first and second signals. Support for claim 21 can be found, for example, in Figures 6 and 8, and the accompanying written description.

Claim 21 distinguishes over the combination of White and DePouilly for similar reasons to those already discussed in connection with claims 1 and 4. Claims 22-30 depend from claim 21 and are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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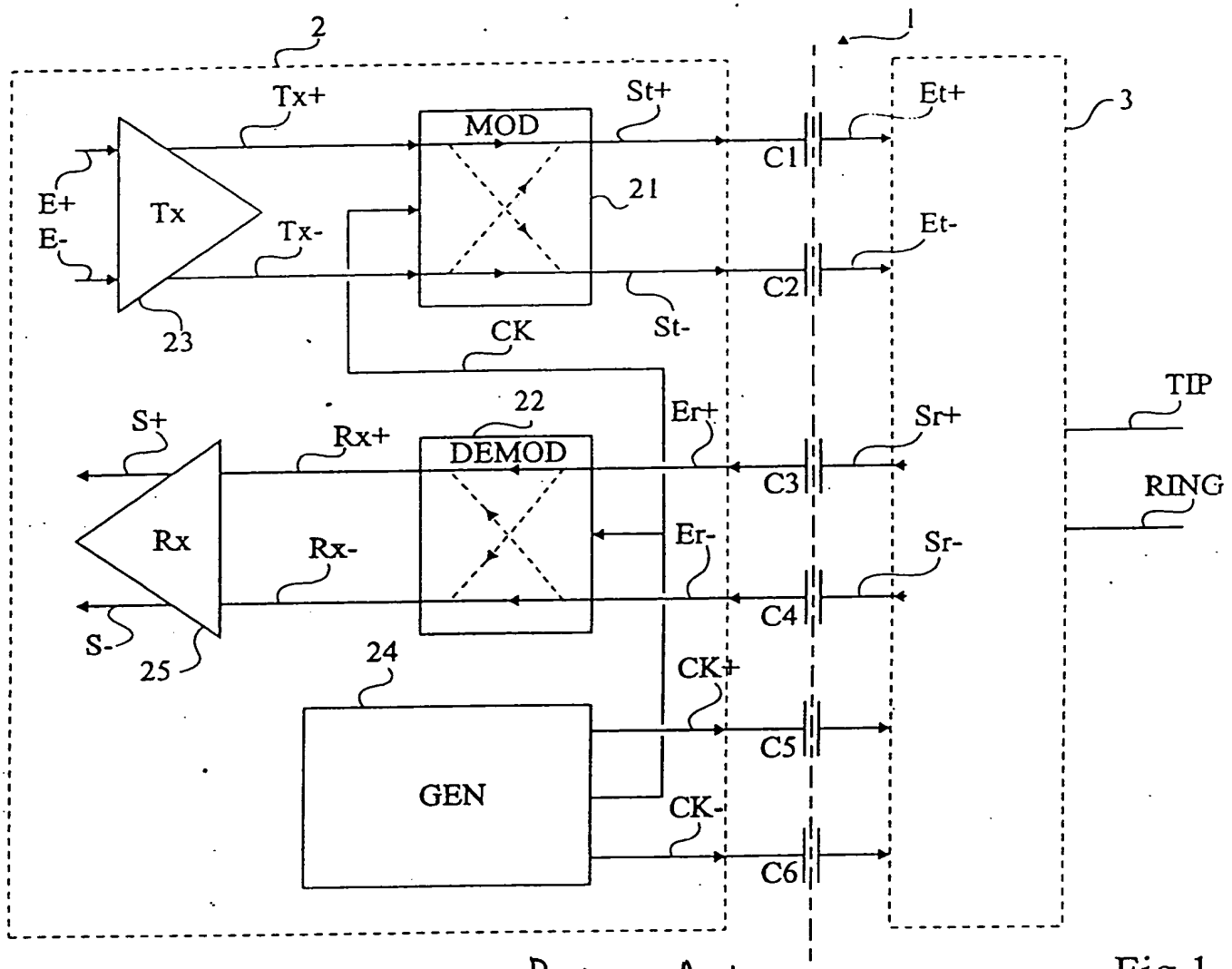
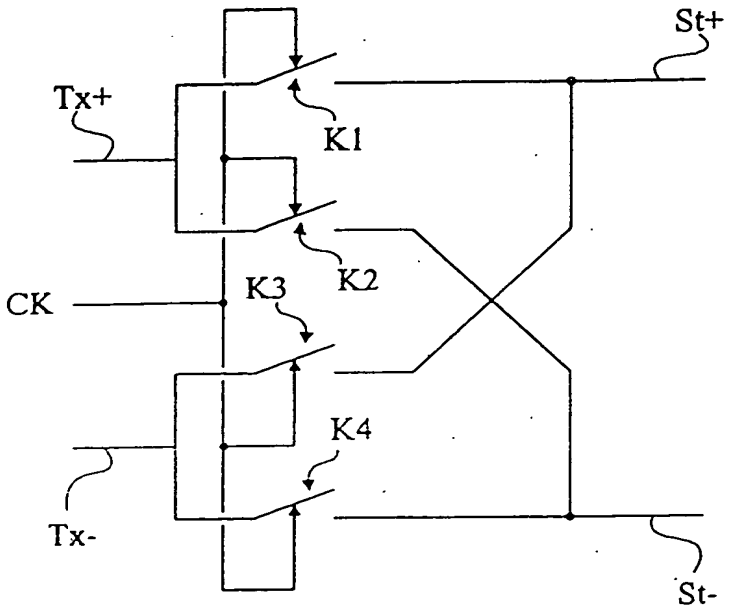
x01/30/2004x



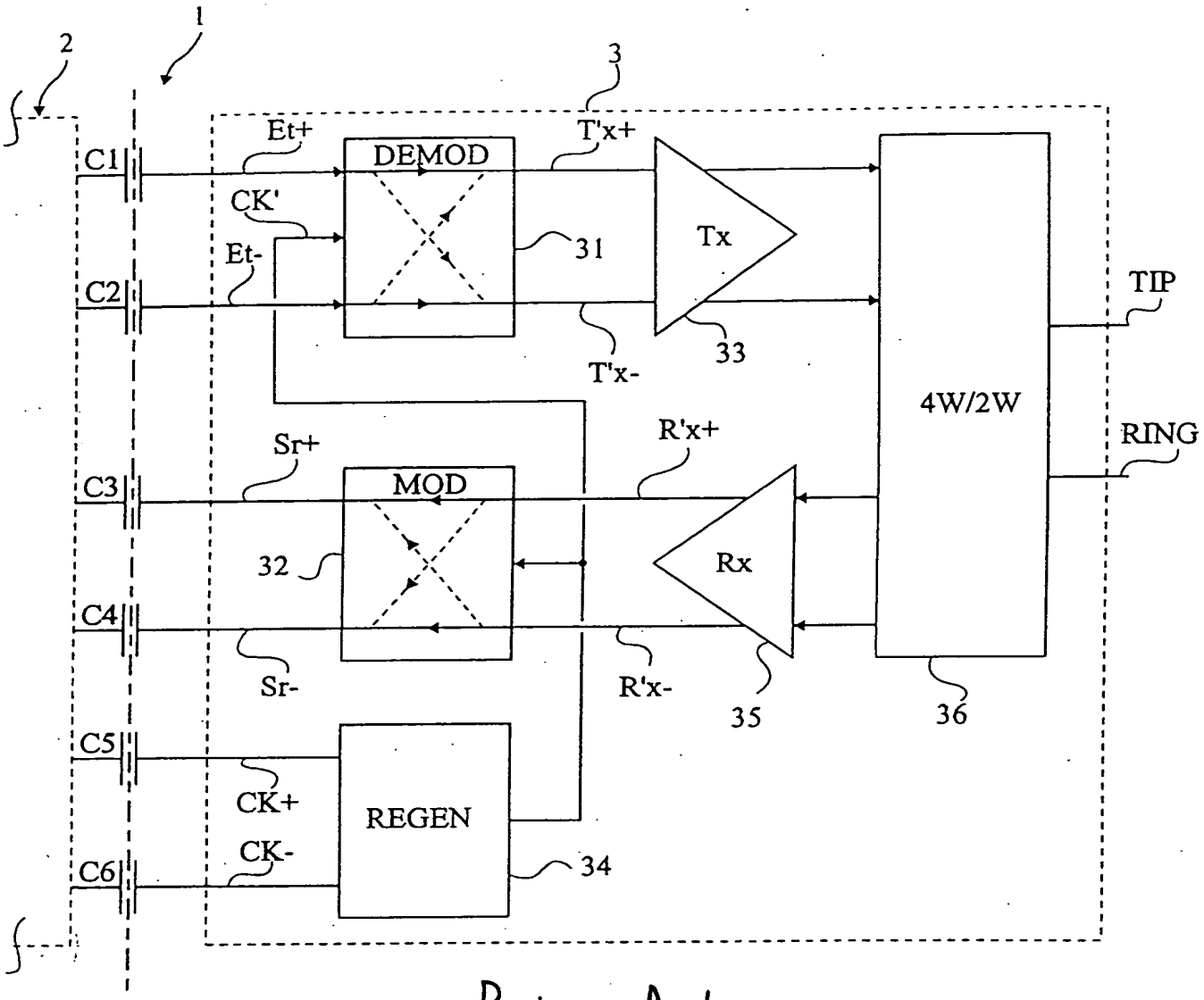
Prior Art

Fig 1



Prior Art

Fig 2

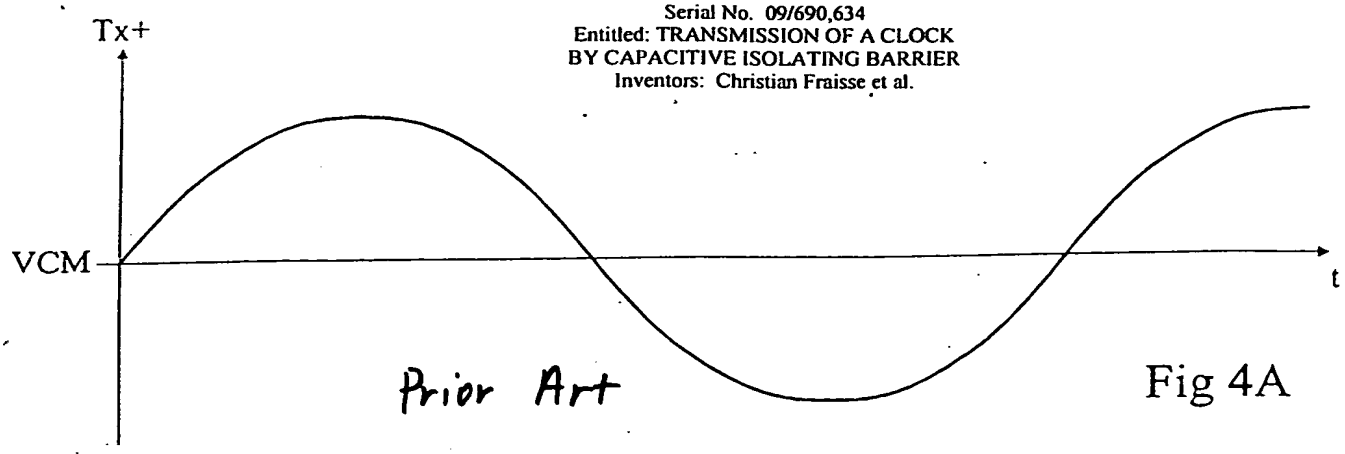


Prior Art

Fig 3

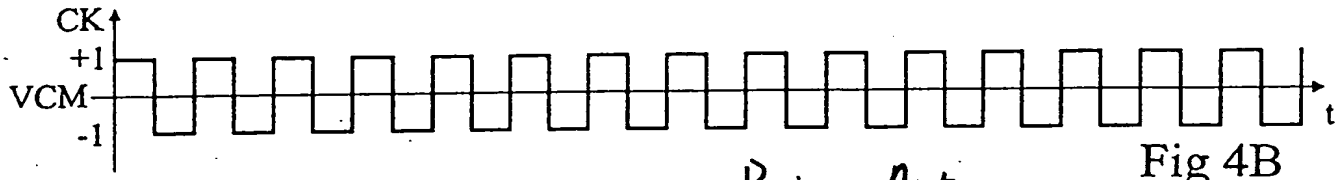
Annotated Sheet Showing Changes

Serial No. 09/690,634
Entitled: TRANSMISSION OF A CLOCK
BY CAPACITIVE ISOLATING BARRIER
Inventors: Christian Fraisse et al.



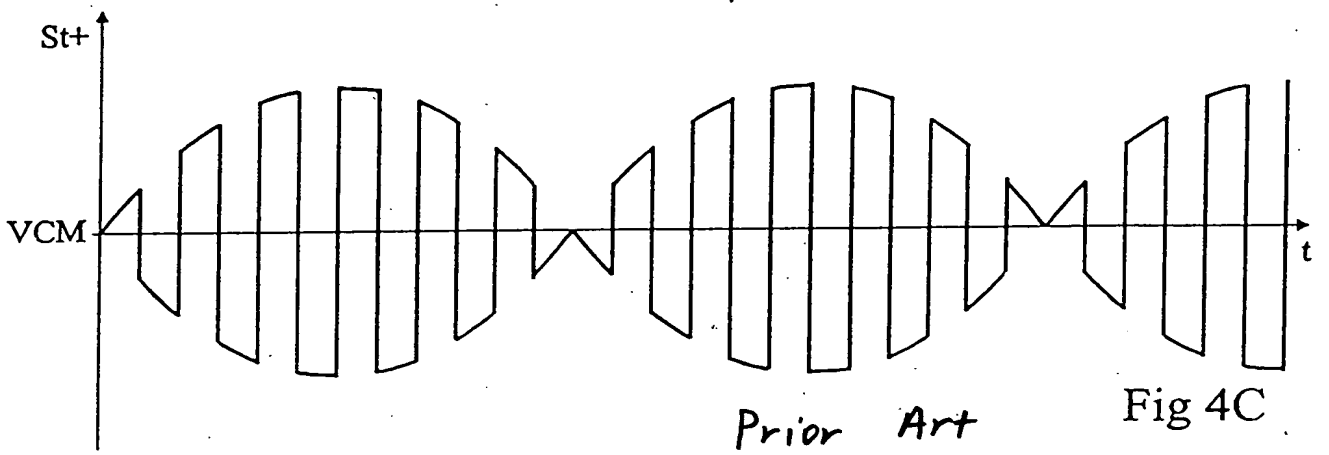
Prior Art

Fig 4A



Prior Art

Fig 4B



Prior Art

Fig 4C

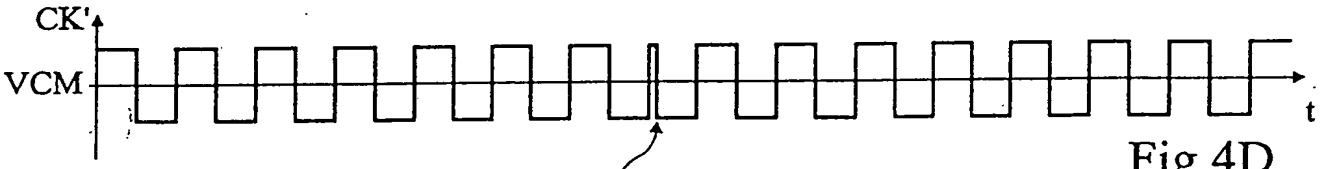


Fig 4D

P

Prior Art

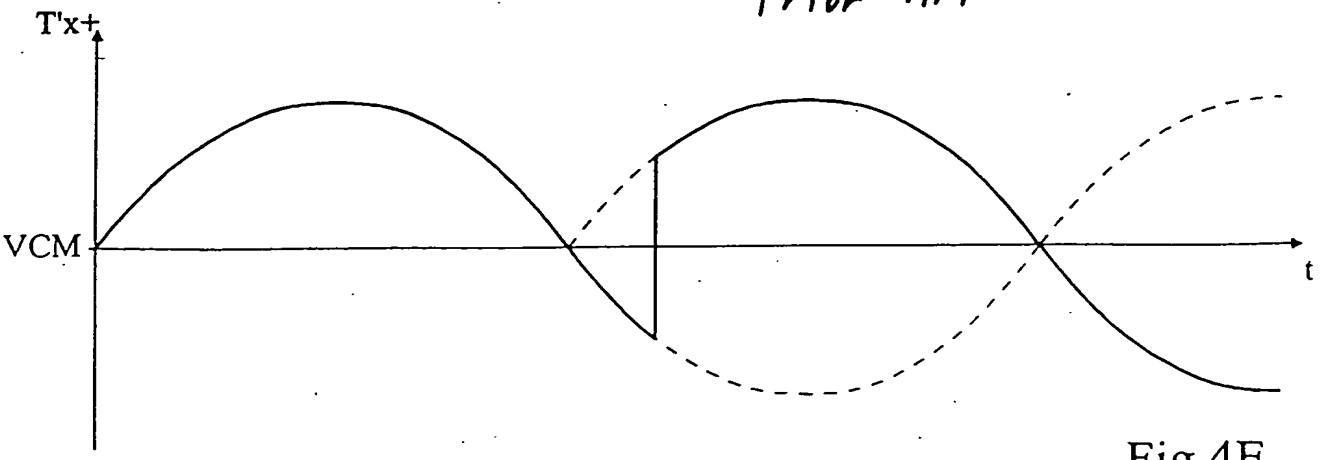


Fig 4E

Prior Art

Annotated Sheet Showing Changes

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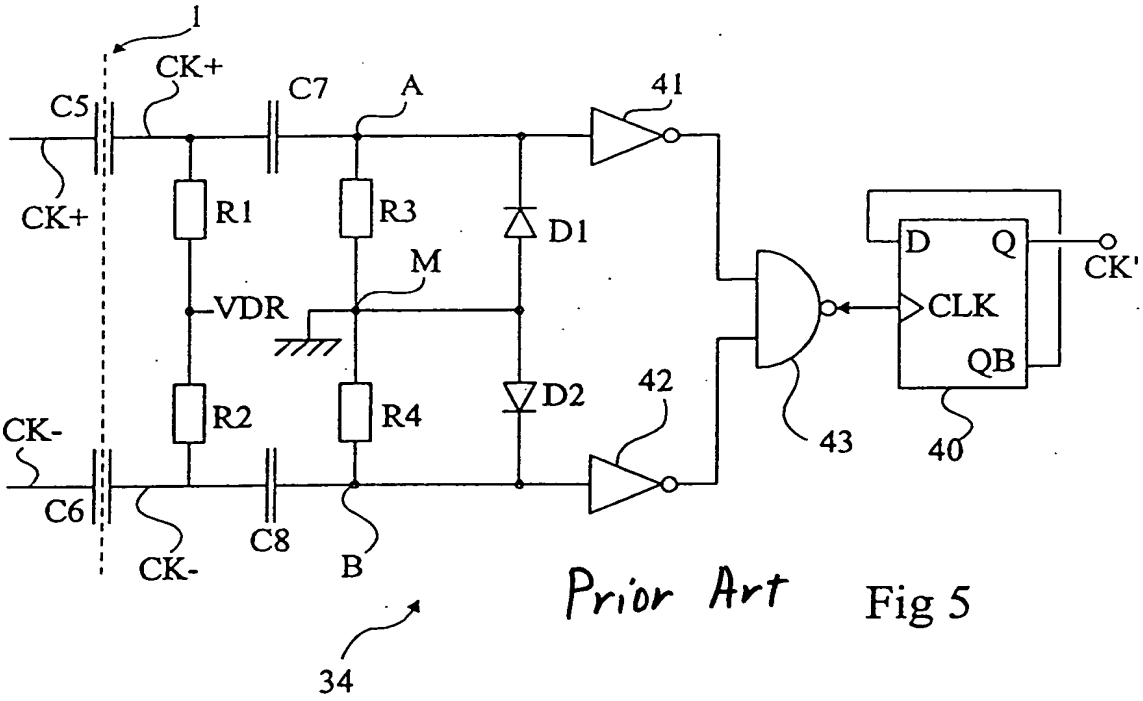
BY CAPACITIVE ISOLATING BARRIER
Inventors: Christian Fraisse et al.



Prior Art

Fig 5

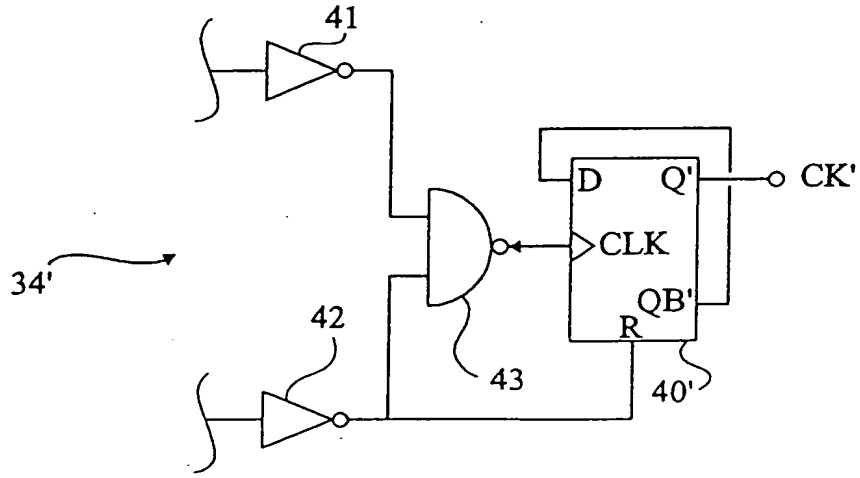


Fig 7